**Proc10A™**

**PCIe x8 (Gen 3) FPGA Computation Accelerators**

**Key Features**
- Altera Arria 10 (GX, SX) FPGAs
- 8-lane PCI Express Gen3 (PCIe x8) host interface
- Dynamically reconfigurable FPGA
- 15 Reconfigurable transceivers supporting multiple protocols and data rates
- Up to 3,036 18×19 Variable Precision Multipliers
- Optional: 1 QSFP suitable for 40 GbE or 4× 10 GbE Ethernet, or single Infiniband QDR link
- Optional: 3 SFP+ cage suitable for 10 Gigabit Ethernet, 8 Gbit/s Fiber Channel, 10-gigabit Ethernet and Optical Transport Network standard OTU2.
- High-Speed Inter-Board connectors (up to 8×14.1Gb/s full duplex GPIO) for board to board and Proc High Speed (PHS) daughter boards connectivity
- Support for Proc High Speed (PHS) Daughterboards, including 8 SATA-3 Interfaces
- 12 general purpose LVTTL External IOs
- Optional: External clock 1 PPS input
- Four level memory structure (32+ GB).
  - Typical sustain throughput of 9,500 GB/s for internal memories and 25+ GB/s for on-board memory as follows:
    - Up to 2,713 M20K (20K-bit) SRAM blocks (53 Mb) with a typical throughput of 9,500 GB/s at 350 MHz
    - Up to 12.7 Mb of Enhanced MLAB (640-bit) SRAM blocks
    - DDR3 1GB 2133MHz on-board memory at 6.4 GB/s
    - 2×DDR3 ECC SODIMMs Banks with up to a total of 32 GB at a maximum sustain throughput of 25.6 GB/s
- Typical system frequencies: 150-450 MHz
- Flexible clocking system
- Low power (8-50W)
- Support for OpenCL™, open standard unified programming
- Supported by Gidel's ProcDeveloper's Kit

**Benefits**
- Leading edge performance and modular flexibility
- Unique development tools reducing the development cycle and simplifying maintenance and upgrade tasks.
- Maintainability, reliability and long-life cycle

**Overview**

The Proc10A system is based on Altera’s newest generation Arria 10 (20 nm) FPGA devices. The Proc10A provides massive capacity (up to 1150K LEs), and high memory and I/O performance. In addition to 8-Lane PCIe gen 3, fifteen 12.5 and 14.1 Gb/s transceivers provide external IOs of up to 200 Gb/s (full duplex). The combination of high-speed direct communication to the FPGA via PCIe, QSFP, SFP+, and General Purpose high-speed transceivers makes the Proc10A ideal for low-latency, high-performance networking and HPC applications. Powerful memory scheme composed of embedded memory with 9.5 TB/s throughput, up to 32 GB ECC DDR III and an additional 1 GB on-board DDR III enables high bandwidth computation and networking, and unique flexibility to achieve diverse algorithm architectures. Using a Gidel or user dedicated add-on daughter boards, the FPGA device can directly interface with standard protocols such as SAS/SATA and customized user interfaces. Eight-lane PCIe Gen. 3 interface allows for strong co-processing between a standard PC operating system and an FPGA based accelerator. The Proc10A system conjoined with OpenCL support and Gidel's ProcDeveloper's Kit maximizes system performance while significantly improving development productivity. Based on this powerful development suite, for over 20 years Gidel has consistently been able to meet unique customer requirements while allowing for flexibility to accommodate long-term product evolution.
Target Application Examples

- DSP (Digital Signal Processing) and HPRC (High Performance Reconfigurable Computing)
- High-speed low-latency networking and network analysis
- Computational Finance and High Frequency Trading
- Data Analytics and Encryption/Decryption
- Life science Applications
- Deep Packet Inspection
- Surveillance, Machine Vision and Imaging
- High performance acquisition systems

Development Environment

The ProcDeveloper's Kit, Gidel's intuitive design and debug environment, facilitates design development effort on the Proc10A system. The kit contains ProcWizard™ Development Application, ProcMultiPort™ and other IPs, Quartus II and USB Blaster.

Based on Altera’s SDK, Gidel supports the OpenCL™ programming model providing means to develop on Gidel’s Proc10A board. OpenCL is a royalty-free, open standard model enabling developers to use C-based language to execute program across heterogeneous systems including FPGAs, CPUs, GPUs and DSPs.

Other high-level design entry options, such as C++, are available via Gidel’s partners.

The ProcWizard performs hardware initialization and automatically generates the following:

- Top-level designs, interface modules/entities and on-board memory controllers for application use.
- Device constraints (e.g., timing, pin-outs and drive strength).
- C++ class(es) application driver(s) enable simultaneous accesses of multiple applications, each to its' dedicated section of the Proc board.
- Interface documentation in HTML or MS Word.

The ProcMultiPort IP and other Gidel memory and data management IPs provide simple and efficient data processing and access to on-board memory. The ProcMultiPort splits the memory into several logical memories, each accessible simultaneously by multiple ports. As a result, the on-board memory is mapped according to the desired algorithm and not vice versa. The main benefits are:

- Simplification of design and enhanced system performance.
- Design compatibility and migration amongst legacy and future Gidel Proc boards.
- Replaces the need for inventory of special memories by using standard field-tested IPs.