**Key Features**

- Stratix III 80E, 110E, 260E, 150L or 340L FPGAs
- 4-lane PCI Express (PCIe x4) host interface
- Five level memory structure (8.5 GB+).
  - Maximum sustain throughput of 3,259 GB/s for internal memories and 10 GB/s for DRAMs as follows:
    - Up to 1040 M9K (9K-bit) DPRAM blocks (1.15MB with 3,000 GB/s throughput @ 300Mhz)
    - Up to 48 M144K (144K-bit) RAM blocks (0.85MB with 259 GB/s throughput @ 300Mhz)
    - Up to 6,750 MLAB (320-bit) RAM blocks
  - A 512 MB DDR2 memory with 4 GB/s sustain throughput using up to 8 ports. (Up to 16 ports with lower access rate)
  - 2 DDR2 SODIMMs with up to 4 GB each at a maximum sustain throughput of 6 GB/s (designed to support future 8GB SODIMMS)
- Onboard SRAM options on SODIMM modules
- Supports 2 PROCe III Daughter Boards: Camera Links, User's Ethernet and other interfaces
- Typical system frequencies: 100-325 MHz.
- Flexible clocking system.
- Volatile and non volatile design security
- Supported by GiDEL’s PROC Developer's Kits

**Benefits**

- Leading edge performance
- Advance development tools
- Low power consumption
- Maintainability
- Reliability
- Long life cycle

**Overview**

The PROCe III™ system provides a high-capacity, high-speed FPGA-based platform fortified with high throughput and massive memory resulting in a powerful and highly flexible system. The PROCe III can be hosted via 4-lane PCI Express. The performance, memory and add-on daughter boards' flexible architecture enable the system to meet almost any computation needs. In addition to 512MB on-board memory, two SODIMM sockets provide up to 8GB of memory or additional connectivity and logic. Abundant memory conjoined with fast PCIe connection enable strong co-processing between a standard PC operating system and the FPGA acceleration. The PROCe III system, with GiDEL's PROCDeveloper's Kit and tools, offers an incredible performance yet supports quick implementation of your unique design. It is done by eliminating the need for a high-speed board design, a PCI Express application driver, board constraints and environment FPGA code. The generated HDL code enables high throughput, easy-to-use parallel access to large memories. As a result, designers can focus on their proprietary value-added design. User designs may be in HDL, C-based, Simulink (graphical design) or any combination of them.
Development Environment

The PROCDeveloper's Kit, GiDEL's intuitive design and debug environment, facilitates design development effort on the PROCe III system. The kit contains PROCWizard™, PROCMultiPort™ IPs, Quartus and USBBlaster, and a PROCHIL™ option.

The PROCWizard performs hardware initialization and automatically generates the following:

- Interface documentation in HTML or Microsoft Word.
- C++ class(es) application driver(s) enable simultaneous accesses of multiple applications, each to its' dedicated section of the PROC board.
- Top-level designs, interface modules / entities and on-board memory controllers for the application use.
- Device constraints (as pin-outs).

The PROCMultiPort core IP provides simple access as FIFOs and frame delays to the on-board DRAM. It enables parallel access to the on-board memory while enabling to split the physical memory into multiple logical memories. As a result the main benefits are:

- Simplifies design and enhances system performance.
- Replaces the need for inventory of special memories by using standard memory and IP.

The USBBlaster enables visibility of internal signals using the available FPGA memory.

**PROCessing Performance examples**

<table>
<thead>
<tr>
<th>Algorithm</th>
<th>Data flow rate</th>
<th>% critical resource of Stratix III logic</th>
</tr>
</thead>
<tbody>
<tr>
<td>1024*1024 FFT</td>
<td>370 MHz</td>
<td>11%</td>
</tr>
<tr>
<td>9*9 filter symmetric 12 bit data 16 bit coefficients</td>
<td>336 MB/s</td>
<td>1%</td>
</tr>
<tr>
<td>7*7 8bit Median filter</td>
<td>255 MHz</td>
<td>11%</td>
</tr>
<tr>
<td>Circle open / close with radius up to 15 pixels 8 bit per pixel</td>
<td>323 MHz</td>
<td>5%</td>
</tr>
<tr>
<td>Threshold, add, subtract, 10Æ8 LUT, &gt;&gt;640 MHz</td>
<td>&lt;&lt;640 MHz</td>
<td>&lt;&lt;1%</td>
</tr>
</tbody>
</table>

* Due to the different resource usage, better utilization is expected in a full design.
* For faster operation, use a multi-channel design.
* For 260 and 340L performance data, contact GiDEL.

**PROCe III board diagram**

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