CoaXPress
Frame Grabber & Image Processing
Upto 12 Channels CXP-6

Overview
The CoaXPress Frame Grabber & Image Processing is based on GiDEL’s ProceV board using Altera’s newest Stratix V FPGA device assembled with at least one PHS_cXp6x4 daughterboard providing 4 to 12 CoaXPress connections. The ProceV flexible connectivity enables tailoring to system requirements such as adding another Camera Link grabbing, adding direct connections to another processing unit in order to split the processing load, etc.

The system’s flexibility conjoined with massive high performance memory enables achieving custom processing needs.

The system development is simplified and enhanced using the ProcWizard Development tool for generating open framework design templates and user application API.

Benefits
- Leading edge performance
- Open framework enabling to achieve application needs
- Unique development tools reducing the development cycle and simplifying maintenance and upgrade tasks.

Key Features
- Support for up to 12 CoaXPress (CXP-6) Channels
- ProceV based on Altera Stratix V GX-A3 up to GX-AB or GS-D8 device enabling user Image Processing and Vision algorithms
- PCIe x8 Gen3 or Gen2
- Stand-alone mode
- Up to 16 GB of DDR3 at up to 19.2 GB/s sustain access
- Optional: 2× 36 or 144Mb DDRII SRAM
- 2 Proc High-Speed (PHS™) connectors for mounting up to two PHS_cXp6x4 or other PHS daughterboards
- 12 general purpose GPIOs
- Support for a PSDB daughterboard that may be used, for example, for Camera Link grabbing or transmitting
- CXP-IEEE 802.3-ba cage with 12 full-duplex transceivers at up to 12.5 Gb/s that may be used for board-to-board / computer-to-computer direct connection, additional acquisition subsystem, high-speed networking, etc.
- Up to 2640 M20K (20K-bit) SRAM blocks (52 Mb) with a typical throughput of 8,000 GB/s at 300 MHz
- Up to 3,926 18×18 Variable Precision Multipliers
- Typical system frequencies: 150-450 MHz
- Flexible clocking system
- Volatile and non-volatile design security
- Supported by GiDEL’s ProcDeveloper’s Kit
- Support for advanced development tools such as Open CL

GiDEL ProceV Board

- 8GB SODIMM
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- 4x transceivers
- 8x transceivers
- HS-C Connector
- HS-B Connector

- PHS_cXp6x4

- Stratix V CoaXPress Protocol + User Logic

- SRAM 36/144Mb (optional)
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- PCIe × 8 Gen3 or Gen2

- Up to additional 8 × CXP-6 or Another PHS daughterboard

- CXP-IEEE 802.3-ba up to 150 Gb IN + up to 150 Gb OUT (Optional)

- 12 transceivers

- External I/Os Connector

- Camera Link In, Out or other interfaces

- 12 GPIOs