For Immediate Release

Gidel First to Market With Application Support Package for Intel's HLS, Offers 5x Faster FPGA Development

Developer tools open the door for software designers to work with FPGAs via HLS, make IP integration and development uniquely fast and easy.

Santa Clara, California, and Or-Akiva, Israel: November 8, 2017 – Gidel, a technology leader in high-performance accelerators utilizing FPGAs, today announced the availability of development tools that take advantage of Intel's HLS, producing a speed increase of 5x over prior development options.

Intel's High Level Synthesis (HLS) compiler turns untimed C++ into Register Transfer Level (RTL) — a low-level FPGA code. Gidel's development tools map board resources to application needs, and provide the glue between the host computer and the FPGA logic by building an Application Support Package (ASP). Gidel's tools provide access for software developers to be able to work with HLS, and simplify integration of new IP that may utilize HLS into existing designs.

Standard HLS does not provide system middleware and board support, but simply accelerates FPGA code development; HLS is intended for traditional FPGA designers. Gidel's development tools grant software developers easy access to the same level of OpenCL design for FPGA by tailoring the ASP(s), using C++ as the programing language. Developers of all types can now work faster and more efficiently, with the freedom to mix between C++ and HDL as most appropriate to the application. For more complex needs Gidel's tools allow for several applications to be accelerated at the same time via the same FPGA by splitting resources between them. Each such part may be developed by a totally separate HLS code.

Gidel has already concluded several successful case studies in FPGA development utilizing its development tools in combination with HLS. "HLS allows for a tremendous speed increase in FPGA development," explains Reuven Weintraub, Founder and CTO of Gidel. "Utilizing Gidel's development tools makes it easy for both software designers and HDL designers to use HLS, according to application needs."

Gidel development tools are optimized for maximum system performance and effective ease-of-use. The generated API maps the relevant user's variables directly into the FPGA design. The on-board DRAM can be split into multiple logical memories accessed in parallel by the users' FPGA code as most optimized to the application need. When the FPGA is used to support multiple applications, each application's API enables it to access only its own variables, thus keeping the system safe from the hardest bugs to find and fix.

Gidel is one of a limited number of FPGA companies selected by Intel to participate in their HLS early access program, and is the first company to announce currently available development tools for HLS.

Visit Gidel in booth 1242 at SC17 in Denver, Colorado (Nov 13-16) for an in-depth presentation, or hear Gidel's talk on "Intel HLS for FPGA with Gidel Development Tools" at the Intel Nerve Center (booth 1203) on Tuesday, November 14, from 2-3pm.

About Gidel

For 25 years, Gidel has been a technology leader in high performance, innovative, FPGA-based accelerators. Gidel's reconfigurable platforms and development tools have been used for optimal application tailoring and for reducing the time and cost of project development. Gidel's dedicated support and its products' performance, ease-of-use, and long-life cycles have been well appreciated by satisfied customers in diverse markets who continuously use Gidel's products, generation after generation. For more information visit www.gidel.com.

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