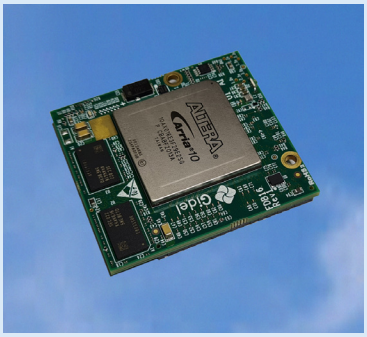
FDB Arria 10 Modules

Ultra-Compact FPGA Modules

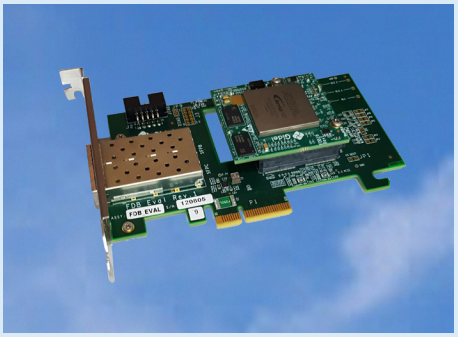
Datasheet

Key Features

- Arria10 FPGA on an ultra-compact modules (49mm x 54mm and 58mm x 62mm - smaller than a credit card)
- Flexible usage via custom carrier card
- Arria10 160, 270 and 660 FPGA:
  - Up to 660K LEs
  - Up to 2,133 M20K DPR
  - Up to 3,374 18 x19 MAC
- Up to 10 GB on-module DDR4 DRAM @ 25.6 GB/s
- Up to 16 Transceivers for aggregate throughput > 230 Gb/s (Rx and Tx):
  - Up to 14 x 14.2 Gb/s (Rx and Tx) 8 can be utilized for 8 x PCIe Gen. 3
  - 2 x 14.2 Gb/s (Rx only)
- FDB I/Os supporting up to:
  - 42 x 3.0V IOs (24 can be 12 LVDS)
  - 4 x 1.2V I/Os
  - 52 x 1.8V I/Os / 26 x LVDS
- Clock sources
  - Differential input reference clock
  - 322 MHz and 125MHz on-module oscillators (for other available frequencies contact Gidel)
- Programming options
  - Active serial via on-board Flash
  - Passive serial via connector pins
  - JTAG via connector pins
- Supported by Gidel Tools:
  - Proc Dev Kit
  - ProcVision Suite
  - PCIe Developer's Carrier Board
- Flexible stacking height: 5-30 mm



FDB 16/27/66 Module



FDB on a PCIe Carrier Board

FDB series, comprising FDB 16 and FDB 27/66, are the smallest mid-range FPGA modules available on the market, ideal for custom PCIe or stand-alone, size-constrained systems. The FDB modules offer a powerful combination of Intel Arria 10 FPGA with high DRAM performance of up to 10 GB @ 25.6 GB/s, and up to 16 x 14.2 Gb/s transceivers (2 are Rx only) at an affordable price range. The FDB modules are supported by Gidel's DRAM controller enabling: 1. Splitting the physical DRAMs into up to 16 separate logical memories, all operating in parallel. 2. Accessing simultaneously each logical memory by multiple sequential ports, each with its own clock and data width. For example, a 128 MB FIFO may be automatically generated by Gidel's tools utilizing a 128 MB logical memory with a single write port and a single read port.

To reduce risk, development time and time-to-deployment, the FDB modules are supported by state-of-the-art development tools and a PCIe carrier board enabling to start developing immediately the application and FPGA code. For example, a user may start developing an image processing IP using a streaming input from files and sending the IP output to a grabber for display, storage, analyzing, etc.

The FDB modules are ideal for diverse applications, including:

- Embedded systems.
- Compact Broadcast and Image-Processing solutions enabling to grab data from multiple fast edge sensors and to perform image enhancements, processing and compression.

Gidel
Committed to Your Innovation

North America:

1600 Wyatt Drive, Suite 1
Santa Clara, CA 95054
+1-408-969-0389
sales_usa@gidel.com

International:

2 Ha'ilan St., Northern Ind. Zone
POB 281, Or Akiva, Israel 3060000
+972-4-610-2500
sales_eu@gidel.com

www.gidel.com

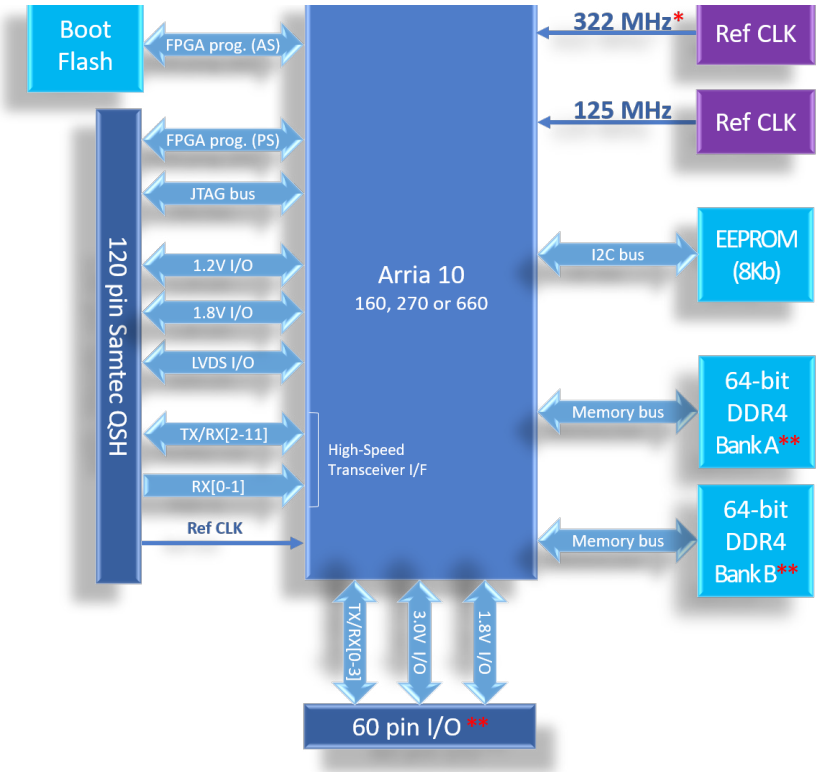
FDB - Ultra-Compact Arria10 Modules

FDB Carrier Boards

The FDB modules have been designed for use with carrier boards to enable tailoring solutions that reduce risks, costs and time to market. User carriers may incorporate any combination of I/Os and configuration schemes. Gidel offers a PCIe developer's carrier board allowing the FPGA designers to immediately begin developing their application and proprietary FPGA design.

Proc Dev Kit and ProcVision Suite

- Enables immediate mapping of board resources to the application needs including tailored host interface and dividing the DRAM into application logical memory units by automatically generating an ASP (Application Support Package) optimized to the system requirements.
- Enables tailoring high-end grabber(s) and Imaging/Vision acceleration flow in an intuitive and simple manner by customizing the ASP, software and the FPGA design code.
- Enables parallel access of multiple applications on the module FPGA thus expediting the development and improving system reliability. For example, firewall and compression may be accelerated simultaneously on the same FPGA and controlled by independent applications.



FDB Block Diagram

* Option for other factory custom frequency

** Bank B DDR4 memory and 60 pin I/O are only available for the FDB27/66 modules. Bank A is 32-bit for FDB66.

Resource	FDB16	FDB27	FDB66
FPGA	Arria 10 160 GX	Arria 10 270 GX	Arria 10 660 GX
DRAM Throughput	12.8 GB/s	25.6 GB/s	19 GB/s
On-board DDR4	2 or 4 GB	10 GB	9 GB
Transceivers	12 (2 Rx only)	12 or 16 (2 Rx only)	12 or 16 (2 Rx only)
Transceiver Speed	Up to 14.2 Gb/s	Up to 14.2 Gb/s	Up to 14.2 Gb/s
I/Os	12x3.0V 4x1.2V 36x1.8V**	Up to: 42x3.0V* 4x1.2V 52x1.8V**	
Dimensions	49mm x 54mm	58mm x 62mm	
FPGA Resources:			
Logic Elements	160K	270K	660K
M20K	440	750	2,133
18x19 MAC	312	1,660	3,374
I/O PLL	6	8	16

Module Resources

* 24 x 3.0V lines can be used as 12 pseudo LVDS pairs

** Each 2 x 1.8V lines may be replaced with a true LVDS pair

Gidel
Committed to Your Innovation

North America:

1600 Wyatt Drive, Suite 1
Santa Clara, CA 95054
+1-408-969-0389
sales_usa@gidel.com

International:

2 Ha'ilan St., Northern Ind. Zone
POB 281, Or Akiva, Israel 3060000
+972-4-610-2500
sales_eu@gidel.com

www.gidel.com