# HawkEye-20G

## 20 Gbps Arria 10 FPGA Computation Accelerators

### Key Features

- Intel Arria 10 GX/SX FPGA, 160/480
- Support for SoC HPS with dual core ARM processors (SX devices)
- PCIe x8 Gen. 3 Express or stand-alone
- Form factor: low-profile
- Low-power, starting at less than 12W
- 2 SFP+ cages
- Cost-effective starting at < $1,000
- Dedicated features that enable tailoring to vertical markets
- Up to 1.2 GFLOPS processing capability
- Multi-level memory structure (18+ GB) Sustained throughput of 128+ TB/s for internal memories and ~16 GB/s for on-board memory as follows:
  - Enhanced MLAB (640-bit) SRAM blocks
  - Up to 28,620 M20K (20K-bit) SRAM blocks (572 Mb) at a throughput of up to 128 TB/s at 450 MHz
  - 2 GB DDR4 on-board memory at a maximum sustained throughput of 5.4 GB/s
  - 8-16 GB DDR4 ECC SoDIMM Bank for maximum sustained throughput of 10.8 GB/s (480 device only)
  - On board user flash (optional)
- Typical system freq: 150-450 MHz
- Flexible clocking system
- Supported by Gidel's Developer's Kit
  - Simultaneous acceleration of multiple applications or processes
  - Unmatched HDL design productivity
  - Simple integration with software applications
  - Data compression and data management IPs
- Supported by Gidel's OpenCL BSP and HLS (I++) ASP based on Intel's SDK (for Arria 10 480 only)

The HawkEye is low profile PCIe accelerator based on Intel's Arria 10 FPGAs. The platform boasts up to 18 GB DDR4 on-board memory, 2 SFP+ links for a maximum of 28 Gb/s, and a PCIe x8 Gen. 3 host interface. The Arria 10 FPGA provides up to 480K LEs and IEEE floating-point capability. The HawkEye's memory scheme comprises embedded SRAM memory with a throughput capability of up to ~128 TB/s, 1-2 GB DDR4, and up to 16 GB of DDR4 SoDIMM (for 480 devices only). The DDR memory may be accessed via up to 48 parallel ports simultaneously.

The HawkEye family includes an option for SoC Hard Processor System (HPS) based on Arria 10 SX devices with an embedded dual core ARM processor. The SoC boards are supported by a MicroSD memory card allowing storage of large program images for stand-alone mode.

The HawkEye accelerator board exhibits an impressive power efficiency, starting at less than 12W. The board is fortified by abundant I/O interface possibilities, including RS422, Opto-coupler, external clock, LVDS, LVTTL (3V), and 30V/0.9A output. The HawkEye can operate as a PCIe-based platform or as a stand-alone compute accelerator. The system has been designed for exceptional high reliability with an MTBF > 1 million hours.

The HawkEye is supported by Gidel's unique proprietary tools for developing on FPGA. The Gidel development tools suite includes Gidel's Developer's kit, data compression and management IPs, as well as Gidel's OpenCL BSP and HLS (i++) ASP.

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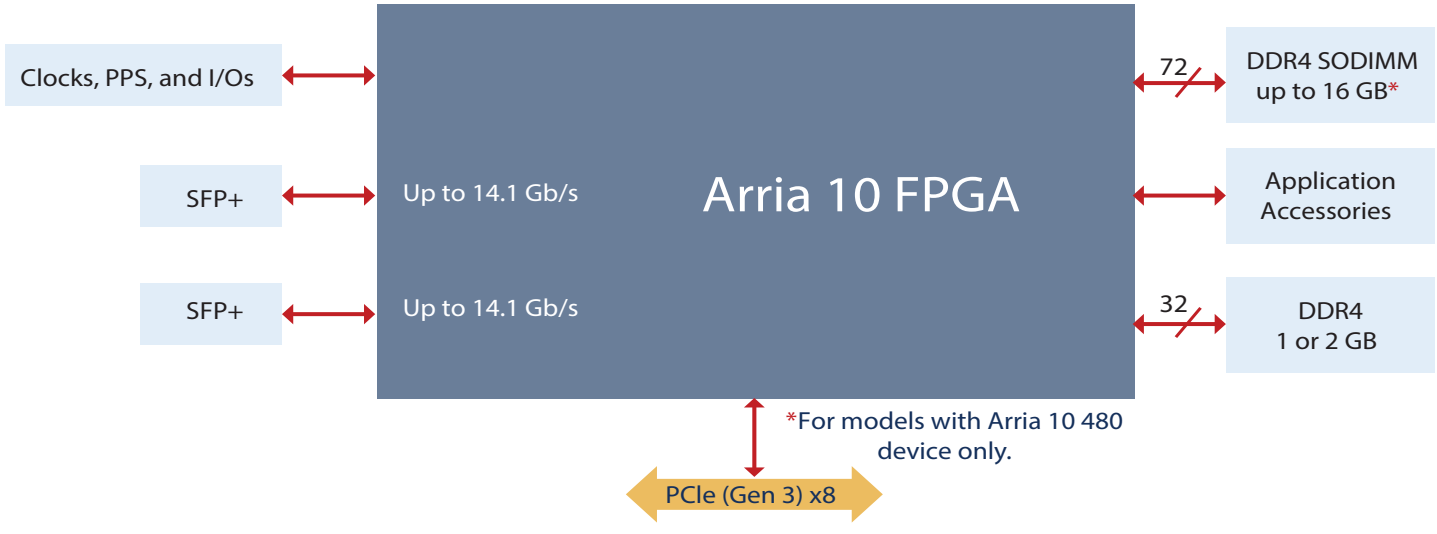
# HawkEye - 20 Gbps Arria 10 FPGA Computation Accelerators

| FEATURE | SPECIFICATIONS |
|---|---|
| **Form Factor** | PCIe low-profile |
| **FPGA** | • Intel Arria 10 GX/SX<br>• SoC HPS with dual ARM cores (SX devices)<br>• 160K or 480K Logic Elements<br>• Embedded 18x19 Multipliers<br>• Embedded M20K and MLAB blocks<br>• 2x 12.5/14.1 Gb/s transceivers<br>• 1.6 Gb/s LVDS performance |
| **Memory** | • Embedded MLAB (640-bit) SRAM blocks<br>• M20K (20K-bit) SRAM blocks<br>• Up to 16 GB DDR4 SDRAM (SoDIMM)<br>• On board 2GB DDR4 SDRAM |
| **Processing Performance** | • Up to 1,431 M20K blocks @ 450 MT/s for total of ~128 TB/s<br>• MLAB blocks@ 450 MT/s<br>• Up to 2 GB DDR4 SDRAM for total of 5.6 GB/s<br>• Up to 16 GB DDR4 SDRAM for a total of 10.8 GB/s<br>• Up to 2,736 18x19 Multipliers |

| FEATURE | SPECIFICATIONS |
|---|---|
| **Host Interface** | PCIe x8 Gen.3 |
| **I/O** | 2x SFP+ |
| **GPIO** | • RS422<br>• Opto-coupler<br>• LVDS and LVTTL (3V)<br>• 30V/0.9A output driver<br>• External clock |
| **Development Tools** | • Gidel ProDev Kit for HDL design flow:<br>✓ Generation of dedicated application driver<br>✓ Splitting of physical on-board memories into logical memories with independent parallel access to/from user logic<br>✓ Generation of environment FPGA code, including all board/IP constrains and user logic wrapper<br>✓ Data compression and data management IPs<br>• HLS (i++) ASP and OpenCL BSP<br>• Intel Tools: Quartus+ QSys and DSP builder |




## HawkEye System Block Diagram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