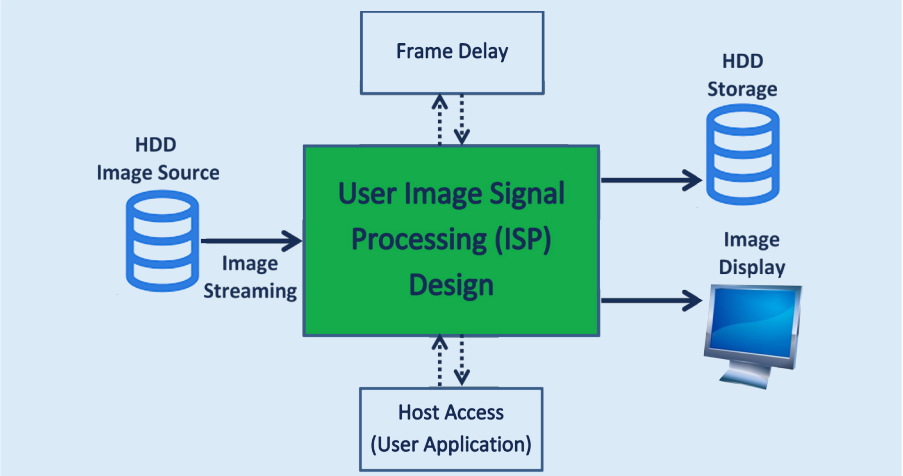
CertifEye Dev Kit

FPGA Image Signal Processing (ISP) Developement and Verification

Key Features

- A complete flow for developing and validating user ISP design, including:
  - Image streaming into user design
  - Grabbing from user design for storage, display and analysis
  - Host access via GUI, macros and user software
- Ideal for design demonstration and evaluation by target end-user
- Image source can be from the host computer's HDD or user application
- IP design is portable to other FPGA devices and technologies
- Flow implemented on single FPGA without the need for additional peripheral connectivity/tools
- Simplicity:
  - Plug-and-play ready for immediate IP development
  - Insert IP design and test
  - Supported by simple design example for hands-on exploration from the start
- Fixable data flow and ability to build other flows such as:
  - Two camera input and a single output
  - Output Vision system information
- Enables developing/validating image processing pipeline with multi-IP blocks
- Supported by Gidel's eco-system:
  - CamSim: camera simulator
  - InfiniVision: multi-camera, multi-image format grabber
  - ProcFG: grabber with powerful image analyzing capabilities and GenICam
  - ProcWizard: enables fully tailoring of grabbing flow and interfacing.
  - Grabbers: variety of grabbers with open FPGA with user image processing pipeline
  - GIL: Gidel Imaging Library (FPGA IPs)



Gidel's **CertifEye Kit** is an optimal solution for developing, validating, demonstrating and evaluating Image Signal Processing (ISP) and pipeline designs on FPGA. In comparison to existing development tools, CertifEye cuts development time by x3 and beyond.

CertifEye is designed to provide a complete and convenient envelop that enables the developer to focus strictly on the proprietary image processing design and its pipeline flow. The entire CertifEye flow is within a single FPGA, without the need for additional peripheral connectivity or tools, and independent of the final target application(s). The CertifEye flow is composed of a camera simulator that streams simulated data to the user ISP and then captures the design's output stream on host computer for displaying, validating, etc.

The CertifEye Kit is virtually plug-and-play enabling the developer to begin at once the ISP design development and validation. A simple design example provides the developer immediate hands-on familiarization with the system flow and supporting tools. The final design can be ported to any Intel FPGA device or other vendors' devices (FPGA or ASIC) by replacing basic libraries. To significantly reduce compilation time, initial design development may be on a small FPGA device and later compiled for the target device(s). The target implementation may use any FPGA board. For a full Imaging/Vision system solution, Gidel offers a number of off-the-shelf grabbers and FPGA accelerators that are designed to utilize these image processing blocks and Gidel Imaging Library (GIL).

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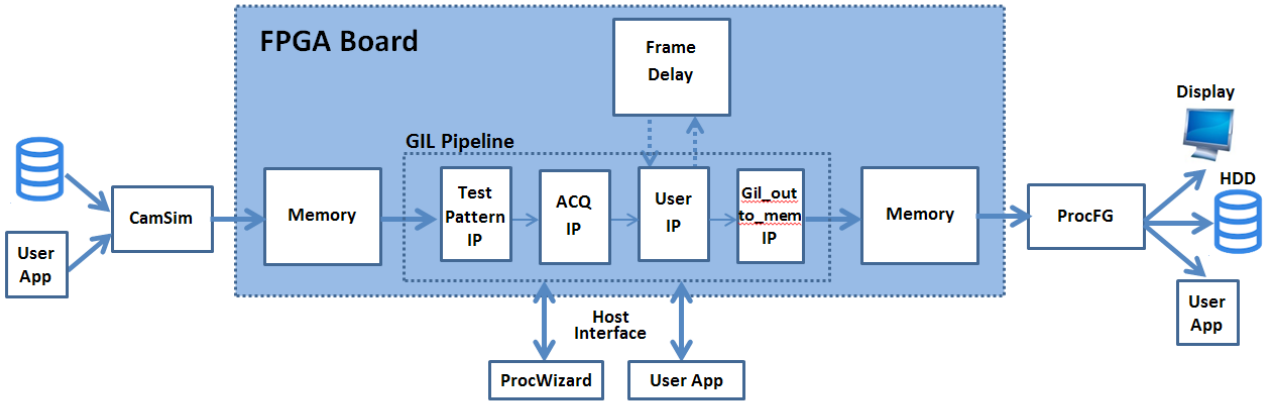
CertifEye Kit Image Signal Processing (ISP) Development and Verification Kit

The CertifEye is designed for both efficient development of the ISP block and the integration of multiple ISP blocks pipelined together. CertifEye enables grabbing from multiple points in the pipeline for displaying and analysis. CertifEye is part of Gidel's comprehensive **ProcVision Suite** that includes a powerful ecosytem for developing a fully integrated Vison and Imaging system. Gidel's ecosystem includes: open grabber boards, unique imaging flows and IPs, development software, GUIs, API and examples.



Example of Image Processing Pipeline

The combination of CertifEye and the ProcVision ecosystem provides the ability to quickly evolve from an ISP design into a fully implemented Imaging/Vision system that incorporates grabbing and image processing, host interface, and integration between the software and hardware. Gidel's development flow has been used by numerous market leaders to enhance the system's features, to improve system reliability and to reduce the development cycle by 50% and even more. Gidel's market-unique solution is a bi-product of over 25 years of close cooperation with its customers to achieve their challenging system requirements within highly demanding time constraints.

PV COMPONENTS	DESCRIPTION
Proc Vision Templates	The Vision Pro templates enable customization such as defining the number of pixels or pixel components per clock and number of bits per pixel. Based on the templates, the flow can be used seamlessly on different Intel FPGA devices, starting from Stratix III and up to Stratix 10 and Arria 10 device families.
CamSim	For image processing development it is crucial to be able to stream large image or video data with the ability to resend the data. The CamSim camera simulator system enables streaming images or video to the user design under test. The images source may be from CamSim's pattern generator or from image files on the hard drive. In addition, the CamSim API can be used to process image streams. For example, incoming images can be processed according to run-time calculated AGC parameters. Based on the CamSim, the system can be efficiently tested, debugged, demonstrated and evaluated. Image formats include: Raw, Mono, Bayer, RGB, RGBA, YUV, YCbCr.
ProcFG	Grabber system enabling to capture the image data stream, perform vision and image processing, and offload image data to the host computer. This grabber flow enables Regions Of Interest (ROIs) recognition by the FPGA processing and user run-time application to grab only relevant ROIs. The ability to grab ROIs reduces PCIe and memory bandwidth usage and enables balancing between the FPGA and host processing. The ProcFG supports GenICam standard and 3rd party image processing libraries via the GenTL.
InfiniVision Mult-Camera Grabber	Grabber system enabling to capture multiple image streams of varying sensors, frame size and image formats. The InfiniVision may synchronize up to 100 cameras. InfiniVision has the capability to grab compressed heterogeneous image data. To further leverage this feature, Gidel offers on-FPGA real-time Lossless and JPEG compression.
ProcWizard	A powerful developer's application for simplifying the development task on FPGA and the integration with the software application. The ProcWizard enables multiple programs to access simultaneously the FPGA, full customization of the software driver, and programmable macros for automatic configuration and flow execution.

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