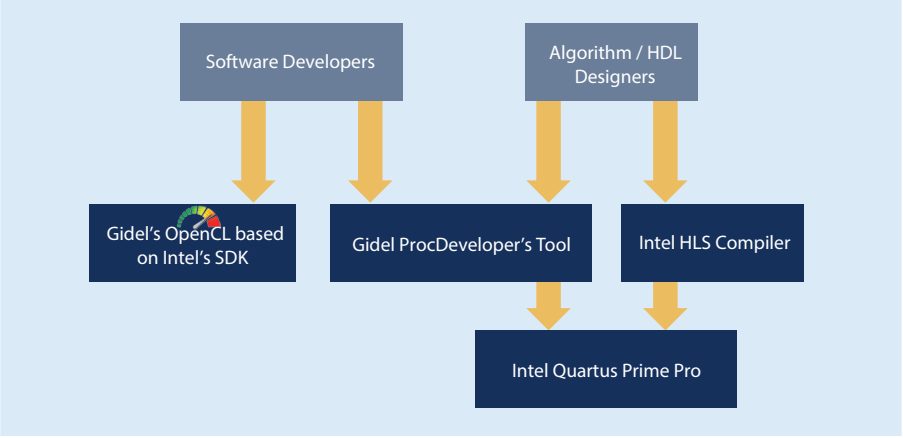
Gidel Developer's Tools

Powerful tools for accelerating development on FPGA

Key Features

- Support for OpenCL based on Intel's SDK, targeting software engineers who want to accelerate applications on FPGA
- HLS Application support package for compiling C++ to HDL, targeting algorithm and HDL designers
- Gidel's Developer's tools for efficient HDL design development:
  - Optimizes system performance
  - Simplifies HDL development tasks and integration with software
  - Automatic generation of HDL envelope and respective software application drivers
  - Generation of PCIe bridge and host interface
  - Debugging tool that directly accesses and controlles the FPGA
  - Ability for multiple programs/ processes to be accelerated concurrently on the same FPGA
  - Memory controller IPs
- Key Benefits of Developer's tools:
  - Dramatically improves project development speed
  - Cuts development cycle time and budget while improving design reliability by enabling on-the-fly debugging
  - Easy maintenance — release a patch within a day
  - No need to spend time on writing documentation
  - Simplifies the interaction between hardware and software developers



Gidel's developer's suite and IPs provide a powerful set of tools and a methodology for simplifying the development task and reducing development time. Gidel's proprietary tools for developing on FPGA offer a market-unique solution that can be used together with Intel's design tools to achieve unmatched development productivity. The Gidel development suite includes the following components:

1. **Gidel's Proc Developer's Kit (ProcDev Kit)** provides an alternative to existing FPGA design methodologies and enables performance to be pushed to the limit. It is easy to use and automatically tailors the process of building the infrastructure required to support algorithm needs by optimizing the use of FPGAs, on-board memory resources, and FPGAs to host communication.

2. **Gidel's HLS Application Support Package (I++)** enables the use of Intel's high-level synthesis (HLS) tool, which takes C++ as input and generates register transfer level (RTL) optimized for FPGA. This tool accelerates the verification time over RTL by orders of magnitude and requires significantly fewer lines of code.

3. **Gidel's OpenCL Board Support Package (BSP)** enables software developers to use the FPGA for accelerating computation. The OpenCL design entry methodology simplifies programming, reducing development time compared with traditional HDL design flow. The bundle provides the means to develop on Gidel's FPGA acceleration boards using C-syntax language.

Gidel
Committed to Your Innovation

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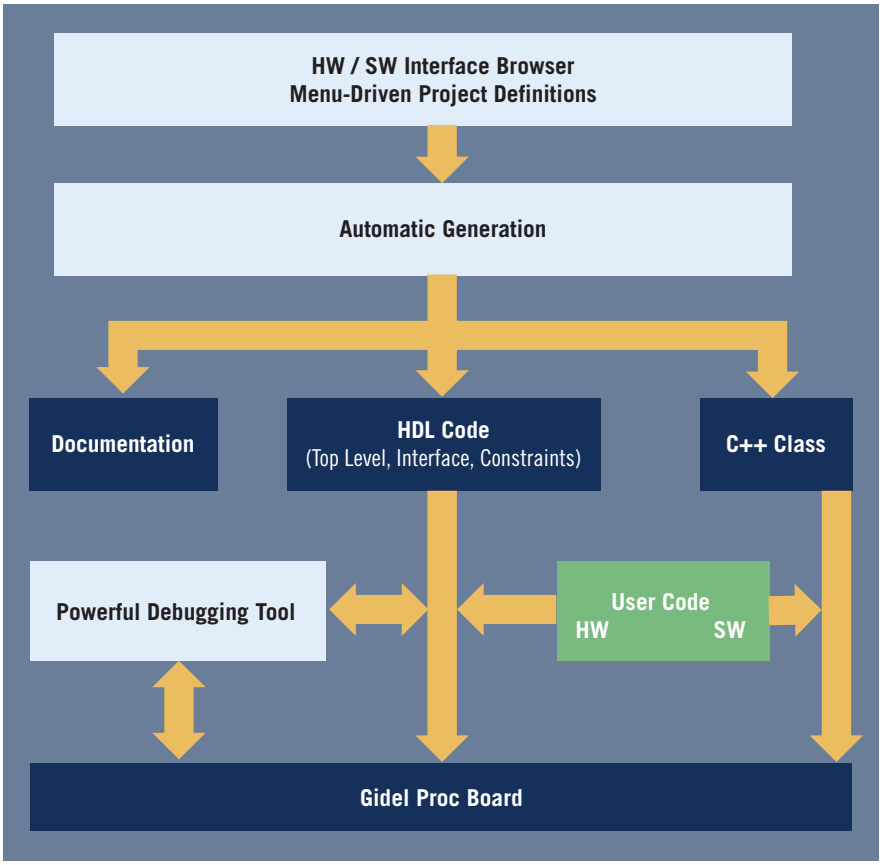

The Gidel ProcWizard Development Flow

- Automatic integration of software and hardware
- HDL code generation (top-level design, PCI interface sub-design, board constraints)
- Automatic integration of Gidel IP cores into the design
- C++ class application driver generation
- Interface documentation generation (HTML or Microsoft Word style)
- Certification of partition generation
- Hardware debugging
- Simple, easy-to-use menu-driven interface
- Automatic hardware initialization and clock setting
- Automatic FPGA loading
- Automatic DMA manipulations

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