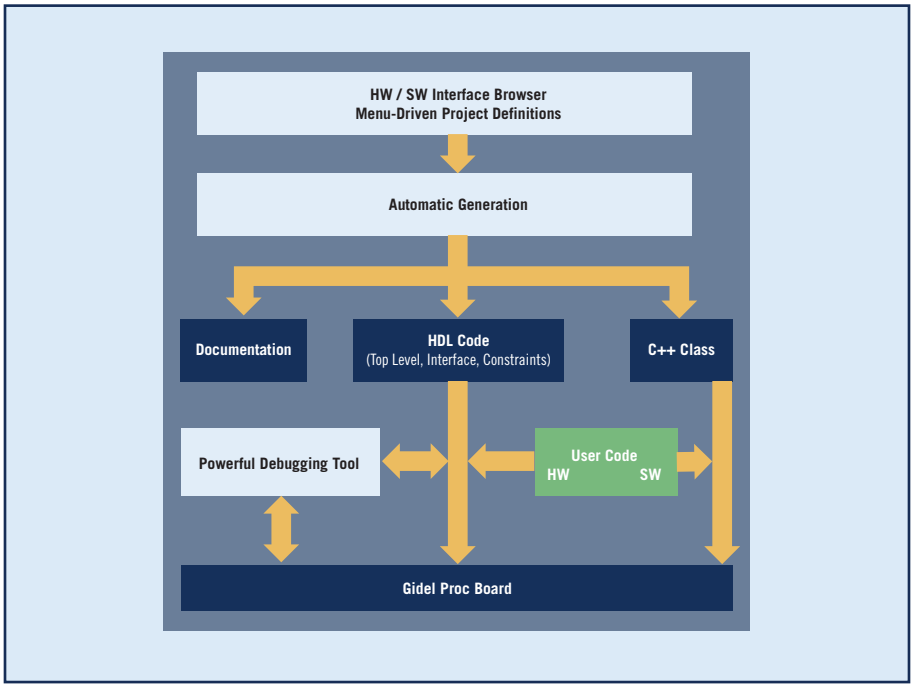
Gidel's Development Tools

Powerful tools for accelerating development on FPGA

Key Features

- Gidel's Developer's tools for efficient HDL design development:
  - Maps the board's resources to the application(s)' needs
  - Generates ASP (Application Support Package)
  - Optimizes system performance
  - Enables seamless integartion of Gidel's memory and data processing IPs.
  - Automatic recognition of active IPs on the FPGA
  - Simplifies HDL development tasks and integration with software
  - Automatic generation of HDL envelope and respective software application drivers
  - Generation of PCIe bridge and host interface
  - Debugging tool that directly accesses and controlles the FPGA
  - Ability for multiple programs/ processes to be accelerated concurrently on the same FPGA
- Key Benefits of Developer's tools:
  - Combines maximum performance and ease-of-use
  - Dramatically improves project development speed
  - Cuts development cycle time and budget while improving design reliability by enabling on-the-fly debugging
  - Easy maintenance — release a patch within a day
  - No need to spend time on writing documentation
  - Simplifies the interaction between hardware and software developers



Gidel's developer's suite provides a powerful set of tools and a methodology for simplifying the development task and reducing development time. The suite includes the following components:

1. **ProcWizard** provides an alternative to existing FPGA design methodologies and enables performance to be pushed to the limit. It is easy to use and automatically tailors the process of building the infrastructure required to support algorithm needs by optimizing the use of FPGAs, on-board memory resources, and FPGAs to host communication.

2. **Gidel IPs** provide efficient means for controlling the data path and managing memory resources. Gidel's IPs include the MultiPort DRAM controller, which enables customized multiple parallel data streaming to feed computational processing according to algorithm needs.

3. **API, Examples** and **Templates** enable developing the user application and custom FPGA code. The ProcWizard automatically generates the HDL and C++ code, enabling software and hardware engineers to share the same interface and database and perfrom system integration flawlessly.

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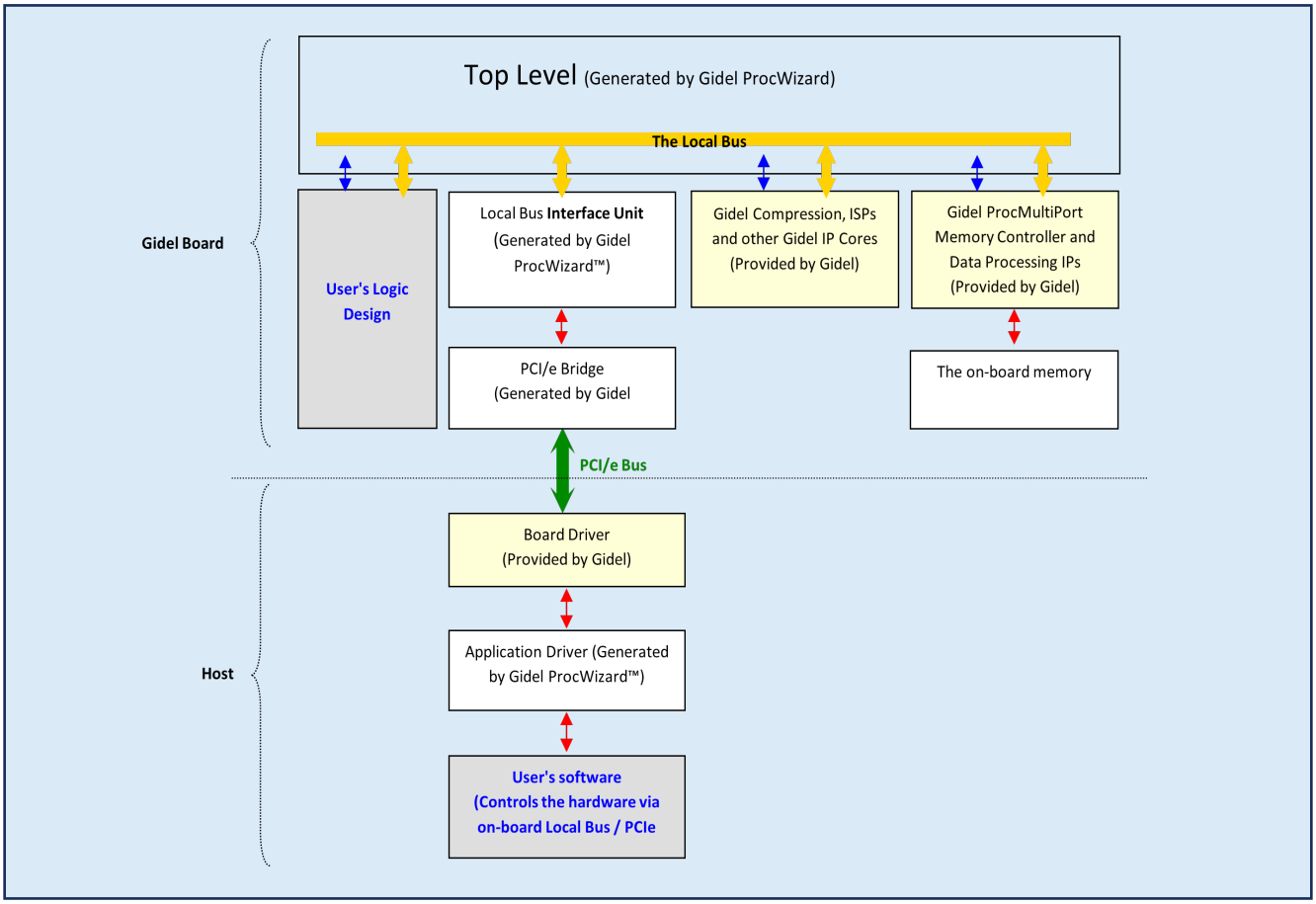

ProcWizard Development Architecture

The Gidel **ProcWizard** automatically generates the HDL, C++ code, and interface documentation, enabling software and hardware engineers to share the same interface and database. The generated software enables seamless communication with the generated hardware design programmed on the Gidel board.

The generated HDL code includes an interface unit, which handles the host communication protocol, memory and data processing IP cores, other IP cores, ISPs that are added to the design, and an envelope for the user's design. A top-level design which connects all these units together is generated as well.

The code may be generated in Verilog, VHDL or AHDL. In addition, the ProcWizard automatically generates the FPGA board constrains for the specific design. The HDL designers need only to connect their design logic to the generated top-level design. The select signals, together with the generated address and data buses, form the Internal Bus, a special logical bus that makes the communication between the hardware and the software very easy to implement.

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